Digital Chip Design (B-KUL-ZA0240)

4 ECTS English 26 Second term Cannot be taken as part of an examination contract

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OC Elektronica-ICT - Campus Geel

Aims

(K1) Basic scientific-disciplinary knowledge and comprehension of the field of industrial engineering

(I1) Problem analysis and solving

(G3) Critical reflection

Objectives:

The student:

Knows MOS device properties and can use them to calculate circuits' behavior.

Knows different circuits for combinational and sequential logic systems and can apply this knowledge to new circuit topologies.

Understands the design flow of digital integrated circuits and knows the principles of CMOS chip fabrication

Can reason on the performance tradeoffs between different logic families and implementations

Knows the design details and interface circuits of integrated memories.

Can analyze the timing performance of a digital circuit, both at circuit and system level.

Can analyze the power consumption of digital CMOS circuits.

Understands the purpose of extra IPs such as IO cells, ESD and PLLs/DLLs.

Previous knowledge

Digital circuit design: combinational and sequential logic systems

Basic electronics, network analysis

Is included in these courses of study

European Master of Science in Radiation and its Effects on Microelectronics and Photonics Technologies (RADMEP) (Geel et al) 120 ects.

Activities

4 ects. Digital Chip Design (B-KUL-ZA5337)

4 ECTS English Format: Lecture 26 Second term

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Content

- MOS Transistor Theory
- CMOS Processing Technology
- Delay
- Power

- Interconnects
- Robustness
- Combinational Circuit Design
- Sequential Circuit Design
- Datapath Subsystems
- Array Subsystems
- Design Methodology and Tools
- Testing, Debugging, and Verification

Course material

Slides on Toledo, own lecture notes

Reading material:

- CMOS VLSI design (Harris) (slides are based on this book)

or

- Integrated Circuit Design 4ed (Harris) (ISBN: 9780321696946)

Language of instruction: more information

De lessen worden gedoceerd in het Engels. Vragen kunnen wel beantwoord worden in het Nederlands.

Evaluation

Evaluation: Digital Chip Design (B-KUL-ZA8240)

Type : Partial or continuous assessment with (final) exam during the examination period

Description of evaluation : Oral

Type of questions : Open questions

Learning material : List of formulas

Explanation

Evaluation is foreseen oral with written preparation unless exceptional events (such as pandemic) do not allow this.

Required in stage	Optional in stage	First term	Second term	Both terms
This year	Next year	Alternating years	External	Prerequisites
Taught by	Language of instruction	Duration		

QUICKLINKS

- Alumni
- International Office
- Student Services
- Pangaea
- LRD
- UZ Leuven
- Jobs and Careers
- Libraries
- News and press
- Agenda
- Culture
- Sports
- KU Leuven shop
- Contact

INTERNAL TOOLS

- Toledo
- KU Loket
- Webmail
- Intranet
- Who's who
- Organisational chart

OTHER LANGUAGES

- Nederlands
- Français
- Deutsch
- Español
- □□□
- Русский

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